What is claimed is:

1. A semiconductor package, comprising:

a board having an upper surface, a lower surface and an aperture;

a plurality of solder bump pads formed on the lower surface of the board;

a plurality of board pads formed on the lower surface of the board;

a plurality of distribution patterns for electrically connecting the solder bump pads to the board pads;

a plurality of contact pads formed on the upper surface of the board, and electrically connected to the solder bump pads;

at least one chip having a plurality of bonding pads, disposed in the aperture;

a plurality of bonding wires electrically connecting the bonding pads to the board pads, at least one end of the bonding wires being bonded to the bonding pads or the board pads by wedge bonding;

an encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and

a plurality of solder bumps formed on the plurality of solder bump pads.

2. The semiconductor package according to claim 1,

wherein the height of each solder bump is greater than the height of the encapsulation part extending over the lower surface of the board.

3. The semiconductor package according to claim 1,

wherein the board is covered with a solder resist except for the regions above

the plurality of solder bump pads, the plurality of contact pads and the plurality of board pads.

4. The semiconductor package according to claim 1, further comprising:

a plurality of via holes formed through the board for electrically connecting the solder bump pads to the contact pads.

5. A package stack including a plurality of the semiconductor packages according to claim 1,

wherein at least one solder bump of an upper package of any two adjacent packages is electrically connected to at least one contact pad of the lower package of the two adjacent packages.

6. A method of manufacturing a semiconductor package, comprising:

forming a plurality of solder bump pads on one surface of a board;

forming a plurality of board pads on the one surface of the board;

placing at least one chip having a plurality of bonding pads in an aperture of the board;

wedge bonding at least one end of a plurality of bonding wires to electrically connect the bonding pads to the plurality of board pads;

encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads on the one surface of the board; and

forming a plurality of solder bumps on the plurality of solder bump pads.

7. The method of claim 6,

wherein the height of each solder bump is greater than the height of the

encapsulation part extending over the one surface of the board.

8. The method of claim 6, wherein at least one solder bump of an upper package of any two adjacent packages is electrically connected to at least one contact pad of the lower package of the two adjacent packages.

9. The method of claim 6, wherein the semiconductor package includes

the board having an upper surface, a lower surface and the aperture;

the plurality of solder bump pads formed on the lower surface of the board;

the plurality of board pads formed on the lower surface of the board;

the plurality of distribution patterns for electrically connecting the solder bump pads to the board pads;

the plurality of contact pads formed on the upper surface of the board, and electrically connected to the solder bump pads;

the at least one chip having the plurality of bonding pads, disposed in the aperture;

the plurality of bonding wires electrically connecting the bonding pads to the board pads;

the encapsulation part provided on the lower surface of the board for encapsulating the at least one chip, the plurality of bonding wires and the plurality of board pads; and

the plurality of solder bumps formed on the plurality of solder bump pads.